



# MS-7297 Ver:0C

## CPU:

AMD K8 AM2 Athlon 64/Athlon 64 FX

## System Chipset:

ATI RS485

ATI SB600

## On Board Chipset:

Winbond Super I/O -- W83627EHG Ver.H

LAN -- RTL8100C/RTL8110SC

HD Codec --ALC861

BIOS --LPC FLASH ROM 4M

## Main Memory:

DDR2 \* 2 (Max 4GB)

## Expansion Slots:

PCI-E X 1 \*1

PCI-E X 16 \*1

PCI 2.3 Slot X 2

## PWM:

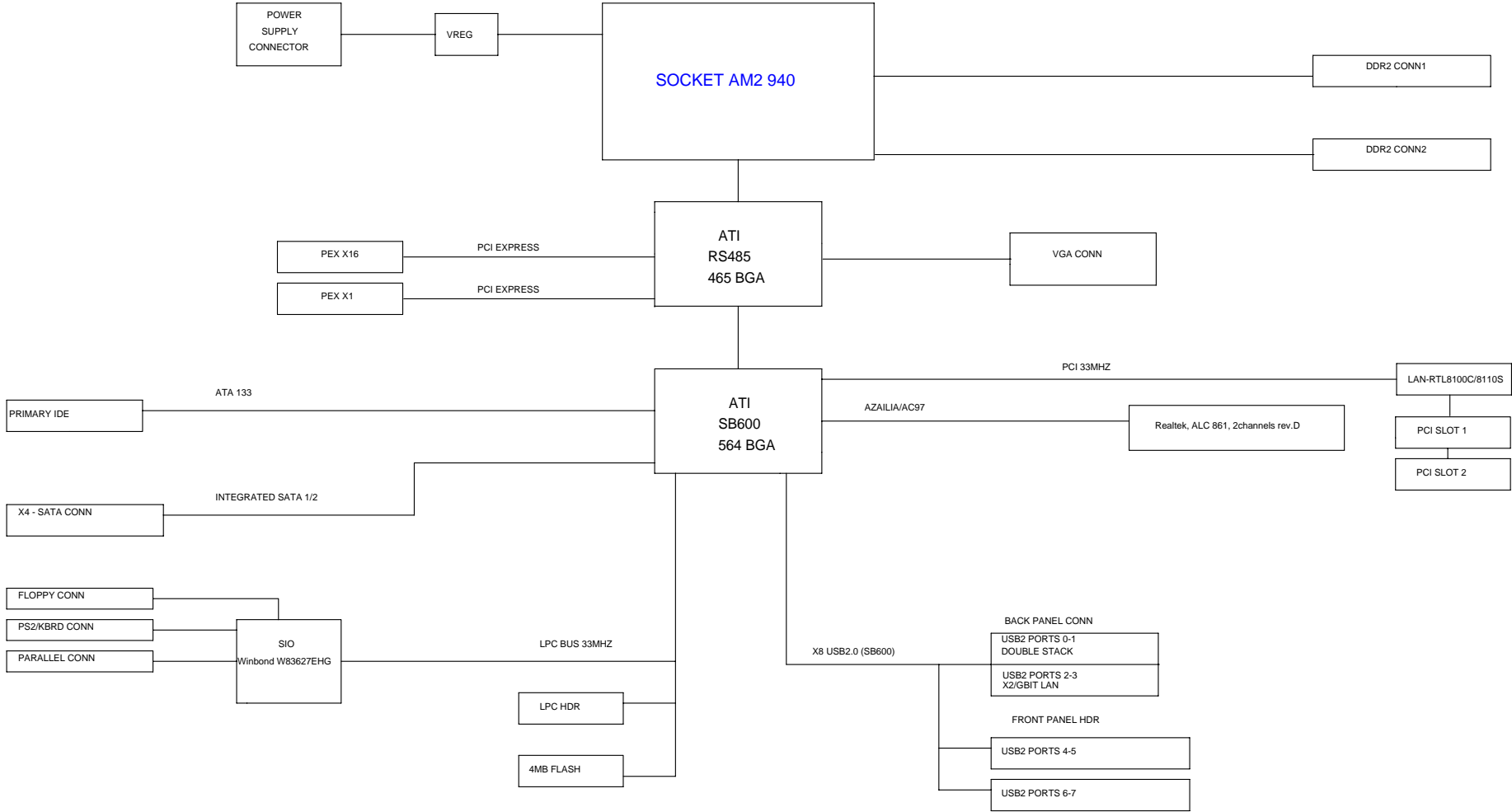
Controller--Intersil ISL6566CR 3 Phase

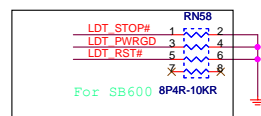
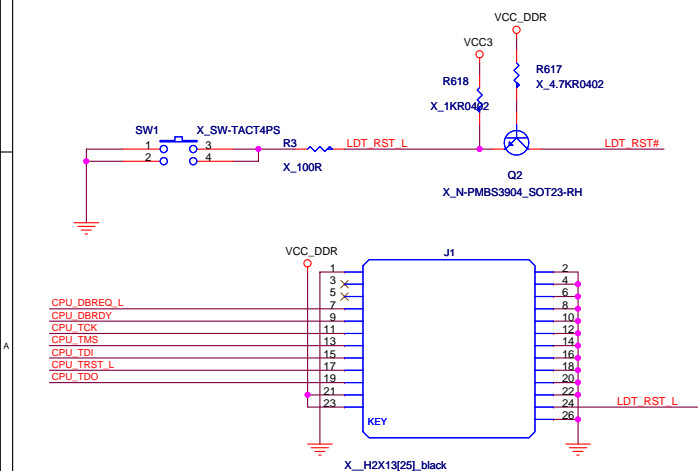
## Clock Generator:

Controller--ICS 951464AGLF

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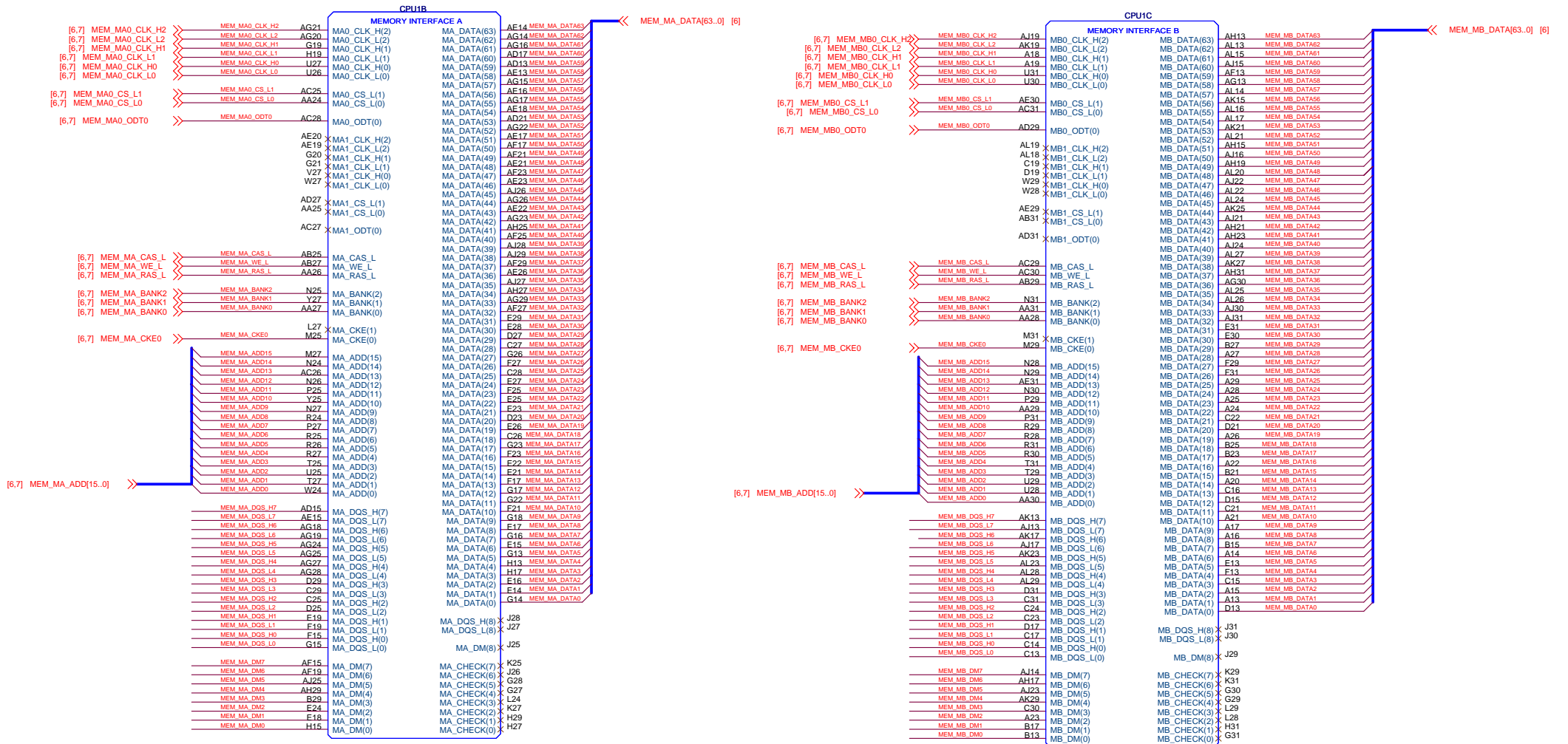
BLOCK DIAGRAM

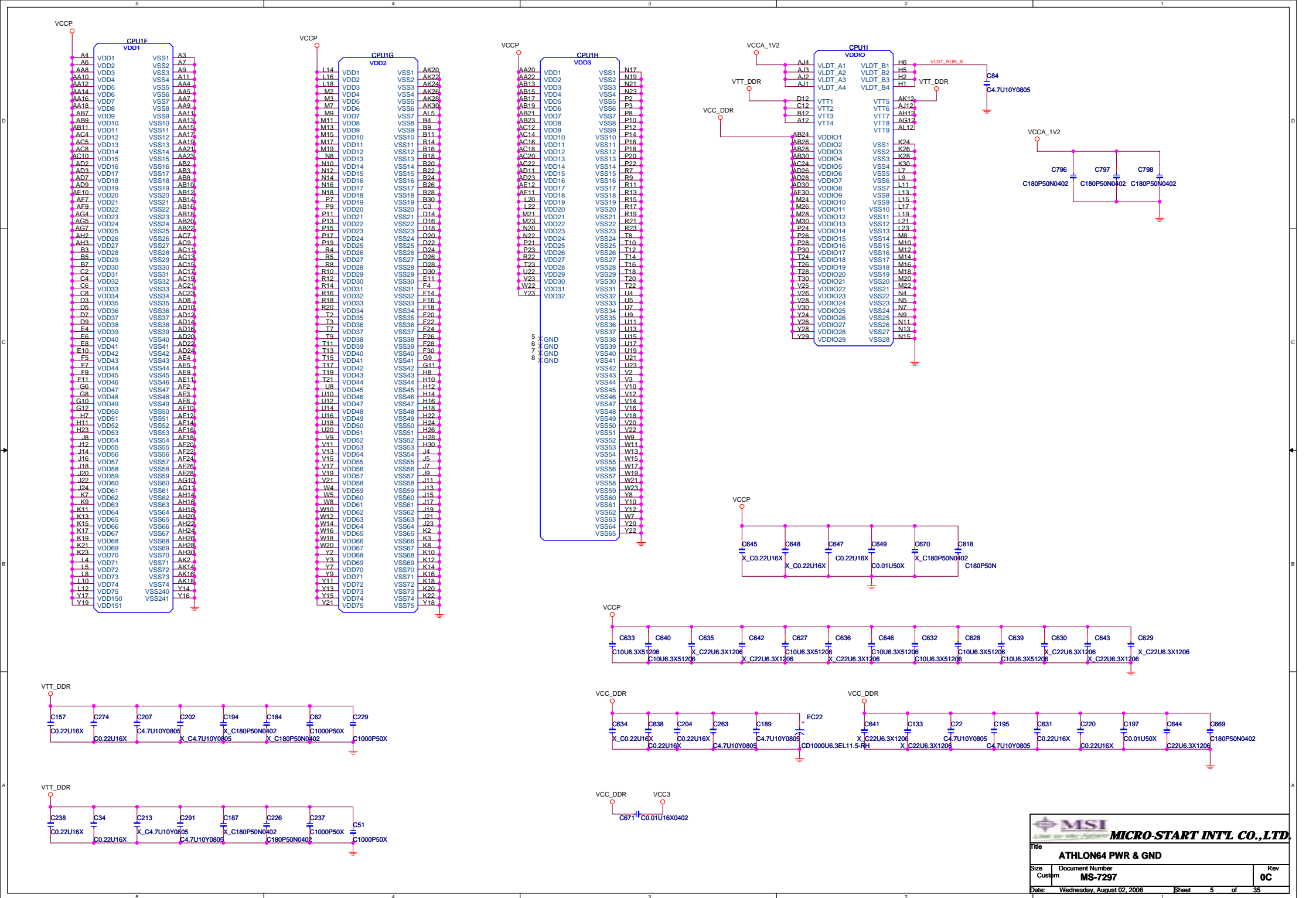




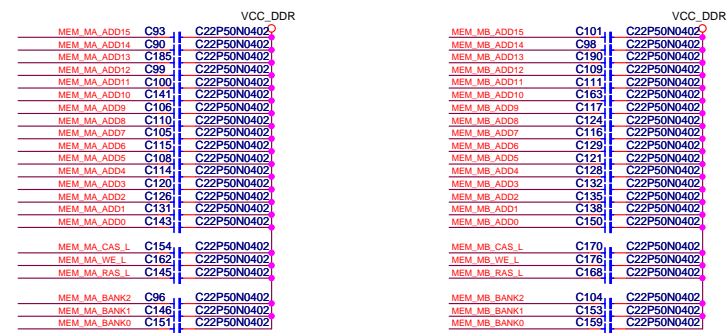
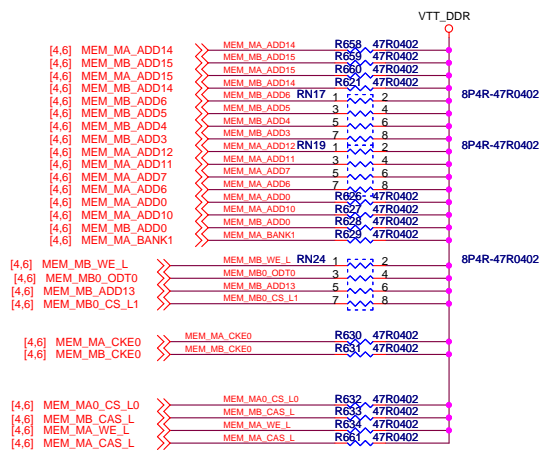
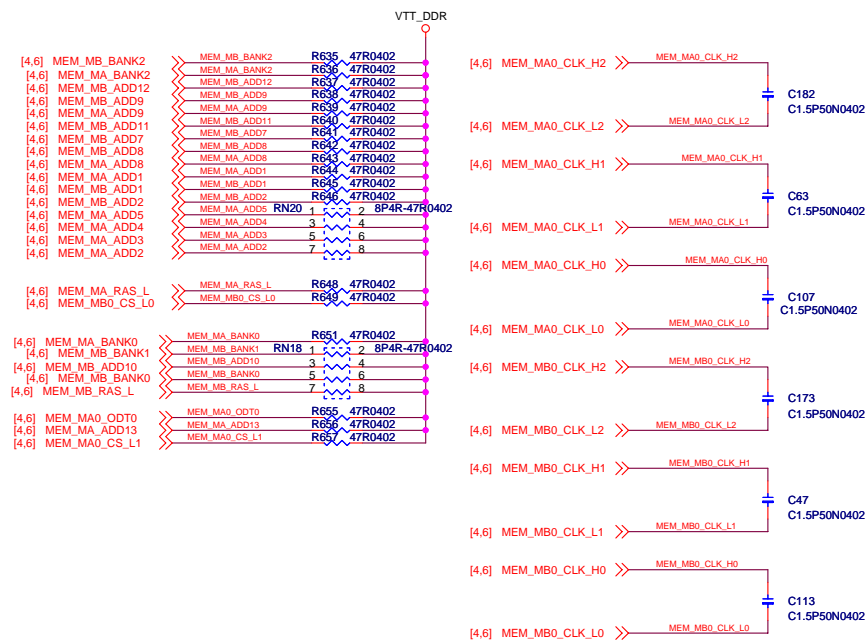
[6] MEM\_MA\_DQS\_L[7..0] >> \_\_\_\_\_  
[6] MEM\_MA\_DQS\_H[7..0] >> \_\_\_\_\_  
[6] MEM\_MA\_DM[7..0] >> \_\_\_\_\_

[6] MEM\_MB\_DQS\_L[7..0] >> \_\_\_\_\_  
[6] MEM\_MB\_DQS\_H[7..0] >> \_\_\_\_\_  
[6] MEM\_MB\_DM[7..0] >> \_\_\_\_\_



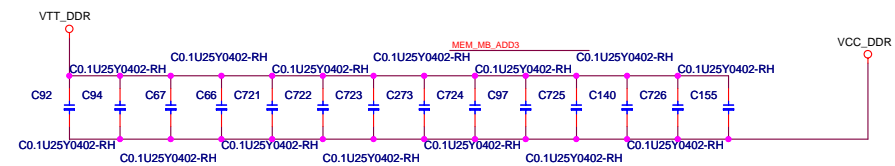
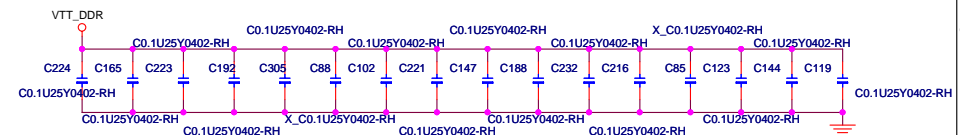




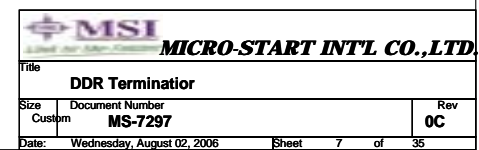
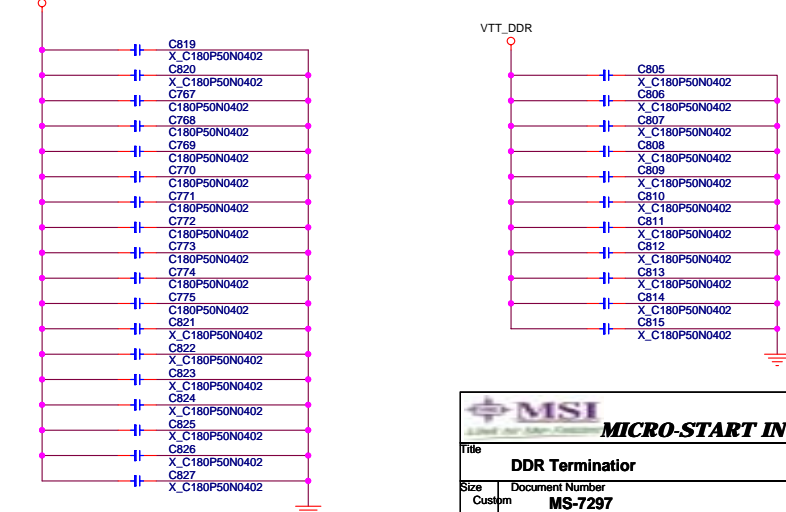


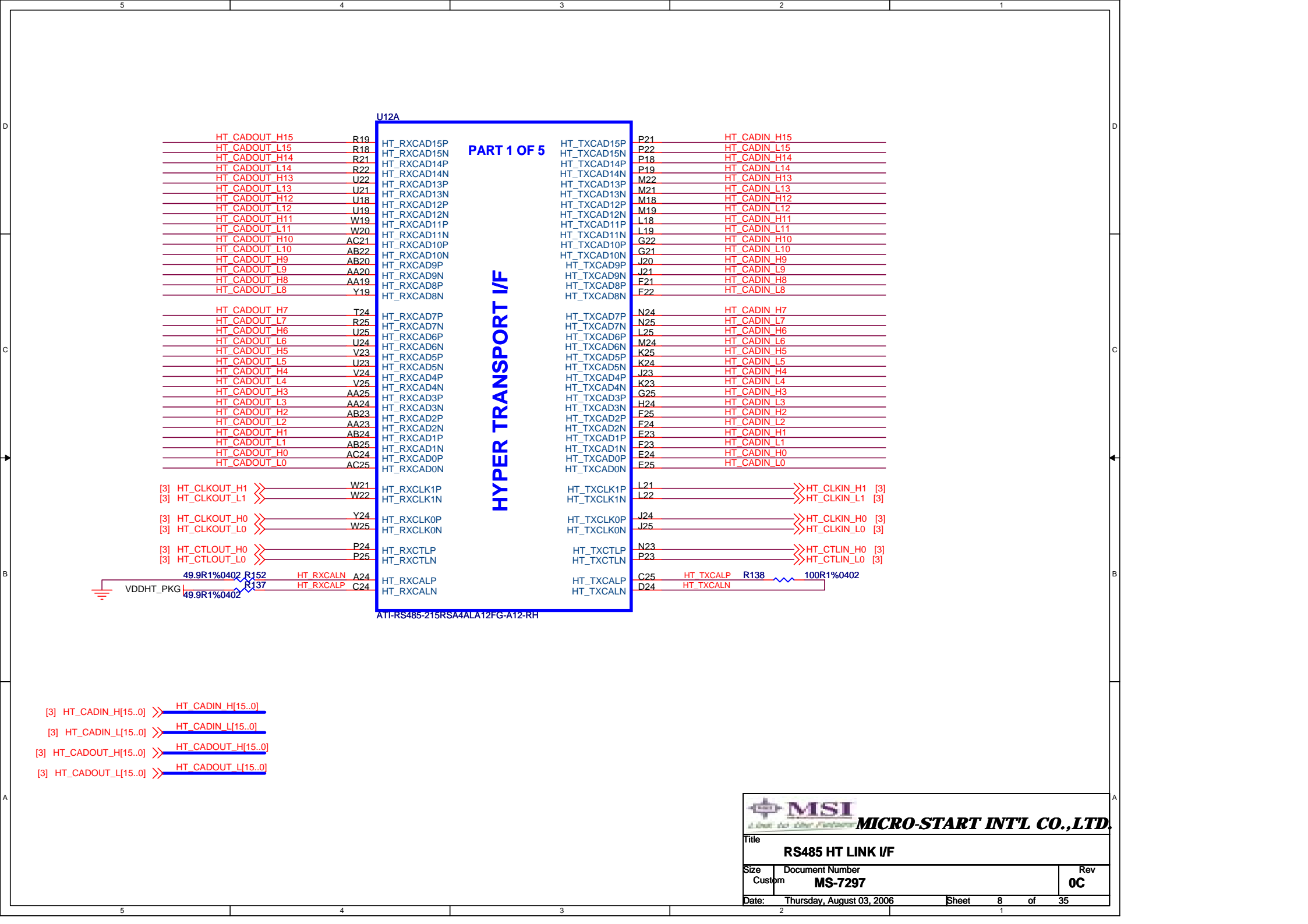
## Decoupling Between Processor and DIMMs

Layout: Spread out on VTT pour

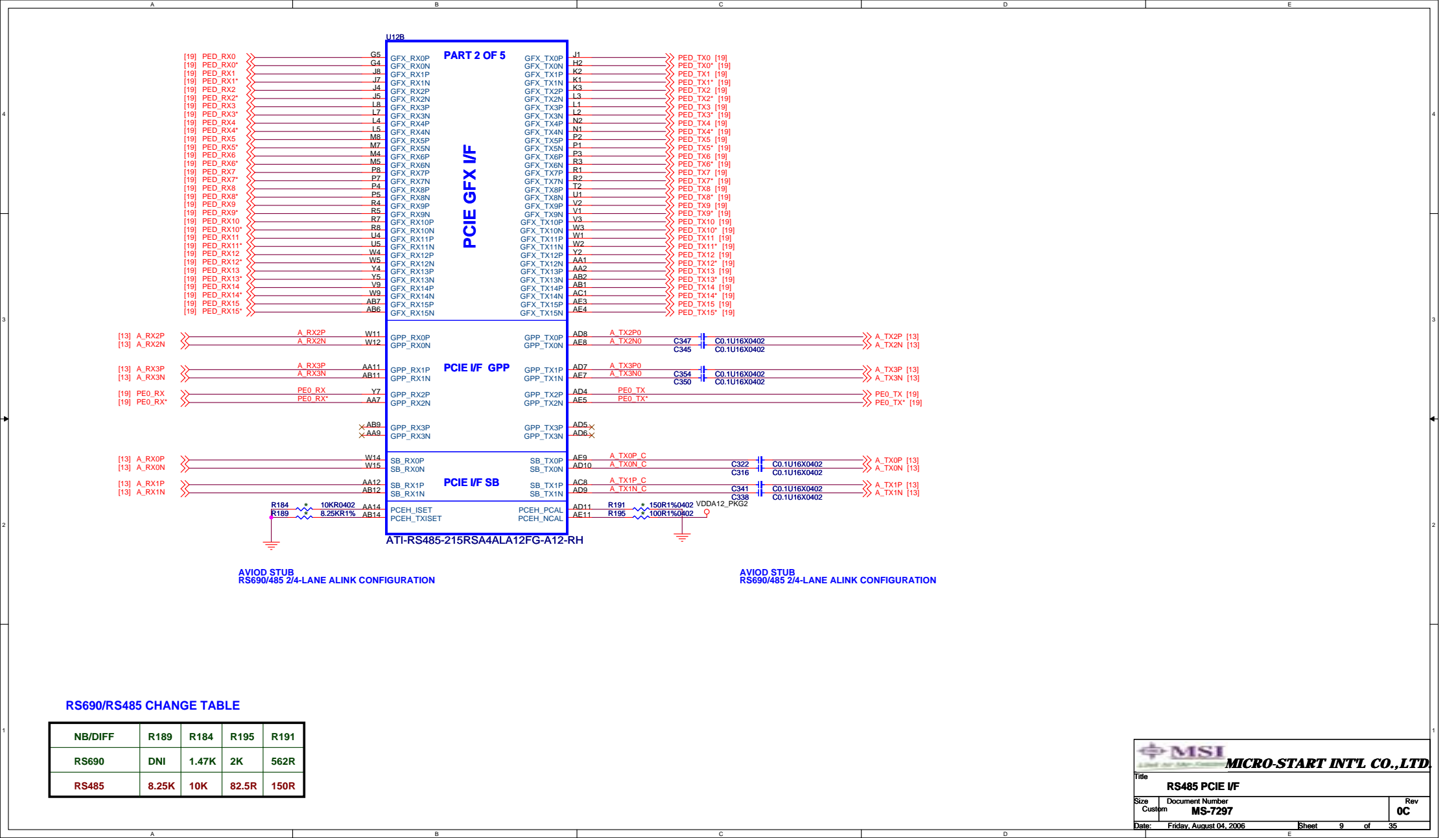


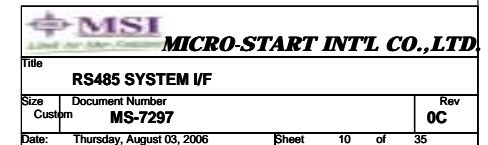
For EMI solution







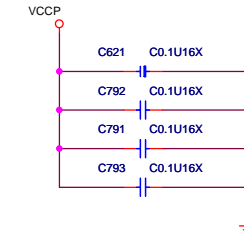




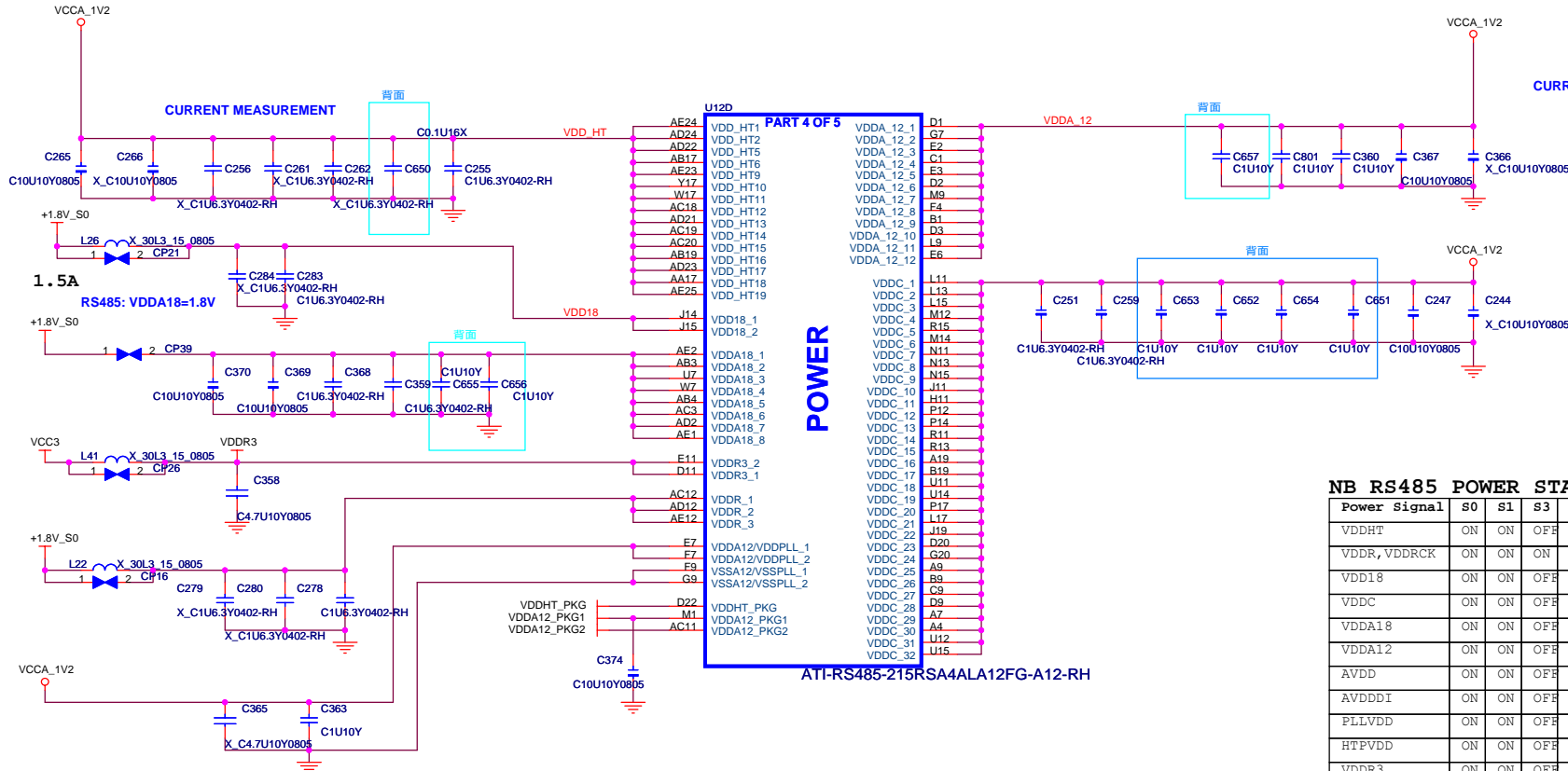
ATI-RS485-215RSA4ALA12FG-A12-RH

GROUND

PAR 5 OF 5

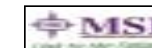


For EMI



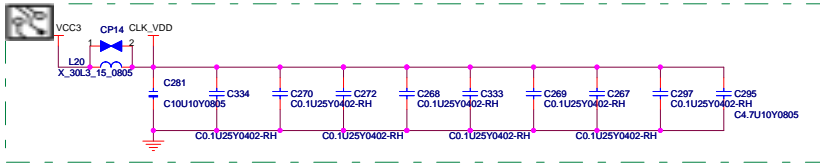
# NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR, VDDRCK	ON	ON	ON	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTFVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



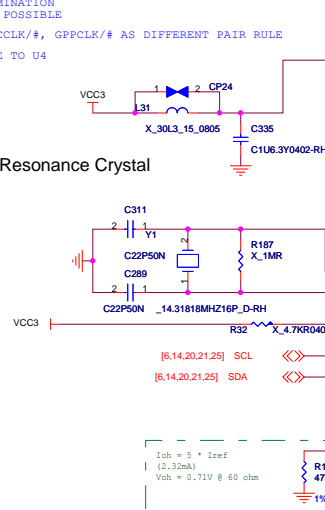
MICRO-START INT'L CO., LTD.

File			RS485 POWER
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- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U4 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U4 POWER PIN

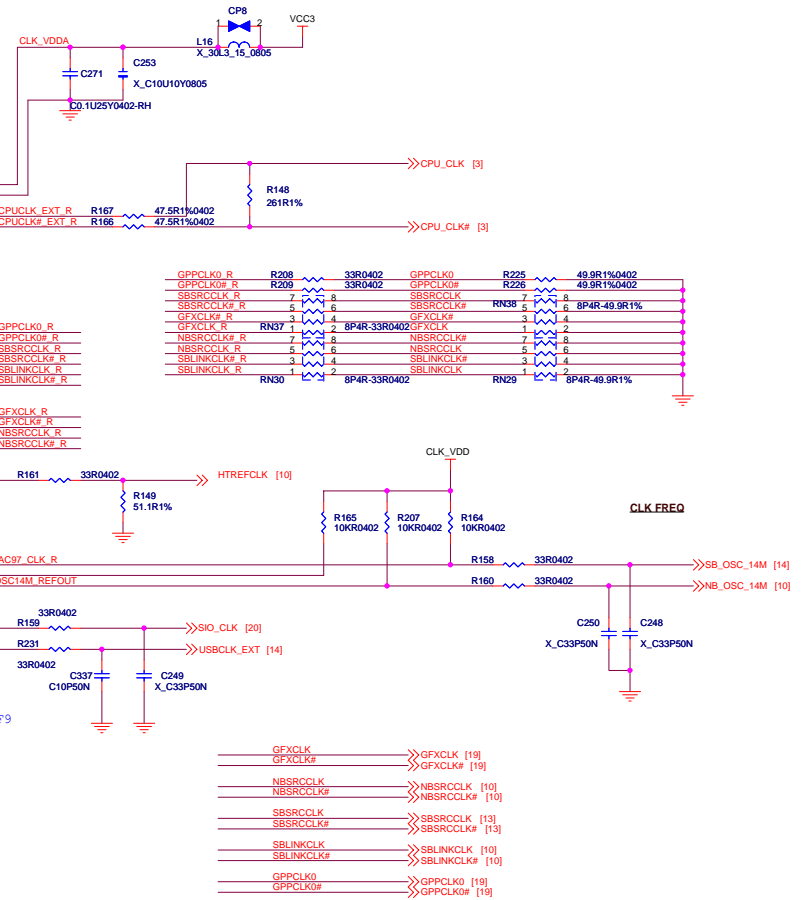
### Parallel Resonance Crystal



I11-5146402-I02 & I11-8460702-SF9

OVERLAP COMMON PADS FOR DUAL-OP RESISTORS

FS2	FS1	FS0	CPU	HTTCLK	SRC	ATIGCLK
0	0	0	Hi-Z	Hi-Z	100.0	100.0
0	0	1	REF	REF	100.0	100.0
0	1	0	230.0	76.7	100.0	100.0
0	1	1	240.0	80.0	100.0	100.0
1	0	0	100.0	66.6	100.0	100.0
1	0	1	133.3	66.6	100.0	100.0
1	1	0	166.6	66.6	100.0	100.0
1	1	1	200.0	66.6	100.0	100.0

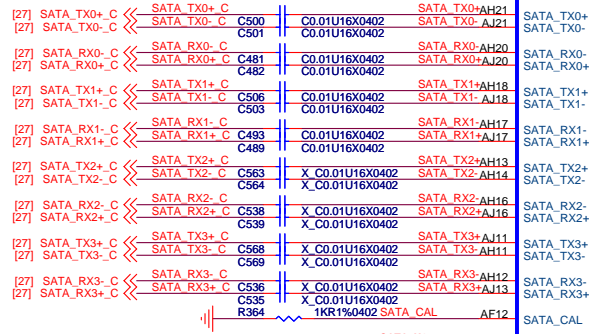




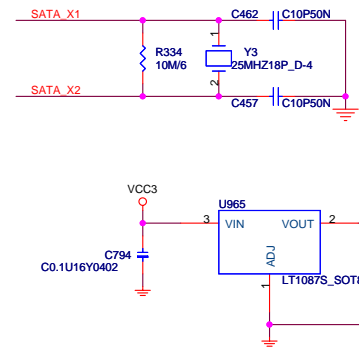




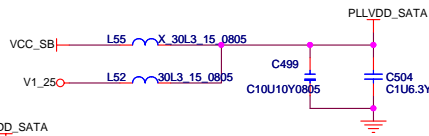
PLACE SATA AC COUPLING  
CAPS CLOSE TO SB600



PLACE R364 CLOSE  
TO U22 BALL  
R364 IS 1K 1% FOR XTAL,  
4.99K 1% FOR INTERNAL CLK

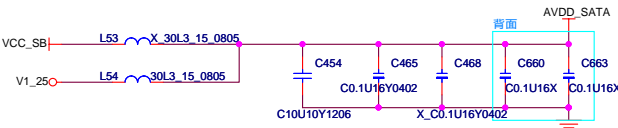


C490 CLOSE TO THE  
BALL OF U22



C499 & C504 CLOSE  
TO THE BALLS OF  
U22

VCC3 = SB600



VCC\_SB = 1.2V for SB600;

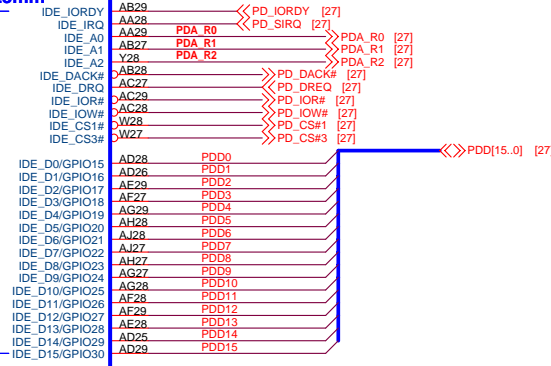
SB600 SB 23x23mm  
Part 2 of 4

SERIAL ATA

SERIAL ATA POWER

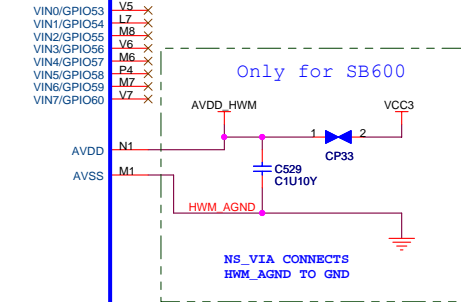
SPI ROM

HW MONITOR



SPI ROM

HW MONITOR



Only for SB600

NS\_VIA CONNECTS  
HWM\_AGND TO GND

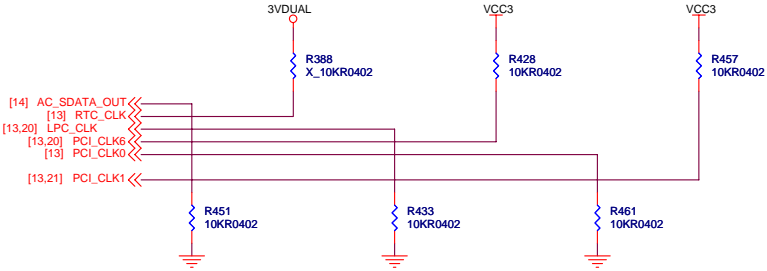




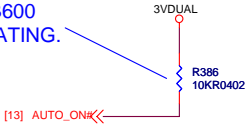


# REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC\_SDATA\_OUT,  
15K PU FOR RTC\_CLK, EXTERNAL PU/PD IS  
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE  
REQUIRED

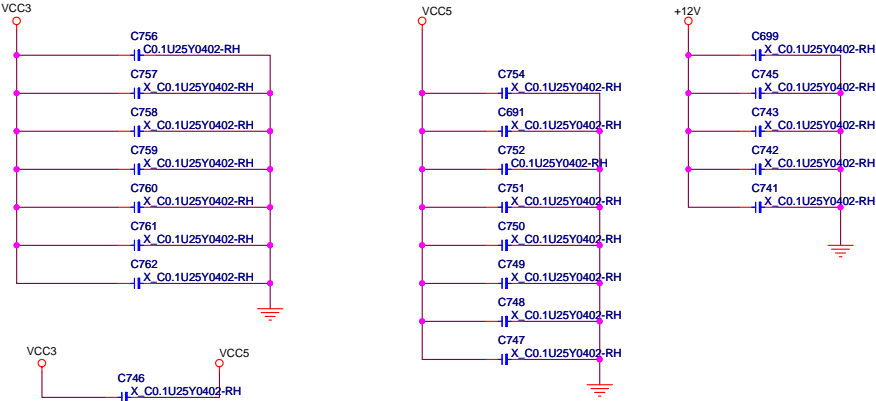


NOTE: R386 PU RESISTOR FOR  
RTC\_IRQ# IS REQUIRED FOR SB600  
TO KEEP THE INPUT FROM FLOATING.

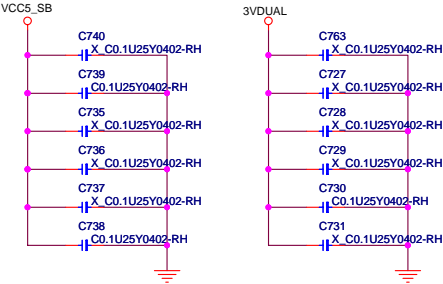


					SB600		SB460	
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	NOTE: FOR SB460, PCICLK[8-7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1-0]			

For EMI



For EMI

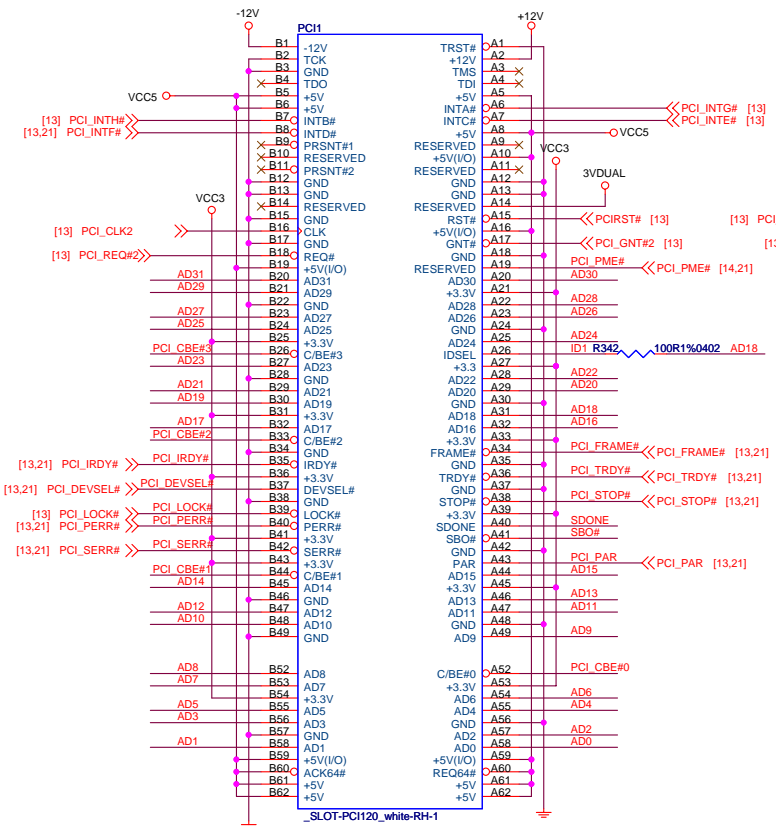


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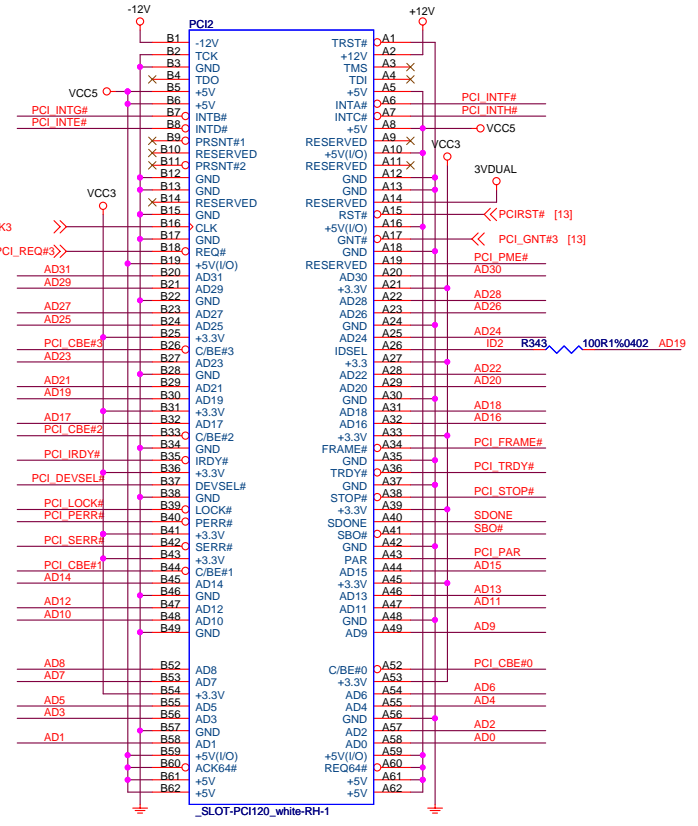
[13,21] AD[31..0] >> AD[31..0]  
[13,21] PCI\_CBE#[3..0] >> PCI\_CBE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



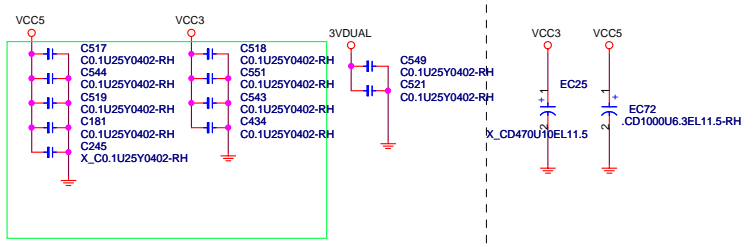
IDSEL = AD18  
MASTER = PCI\_REQ#2  
PCI\_GNT#2

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



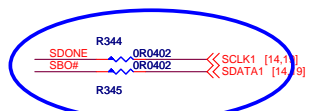
IDSEL = AD19  
MASTER = PCI\_REQ#3  
PCI\_GNT#3

PCI SLOT DECOUPLING CAPACITORS



For EMI

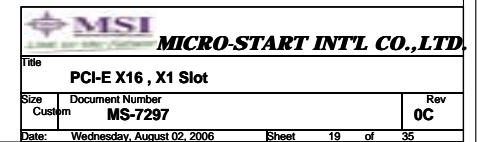
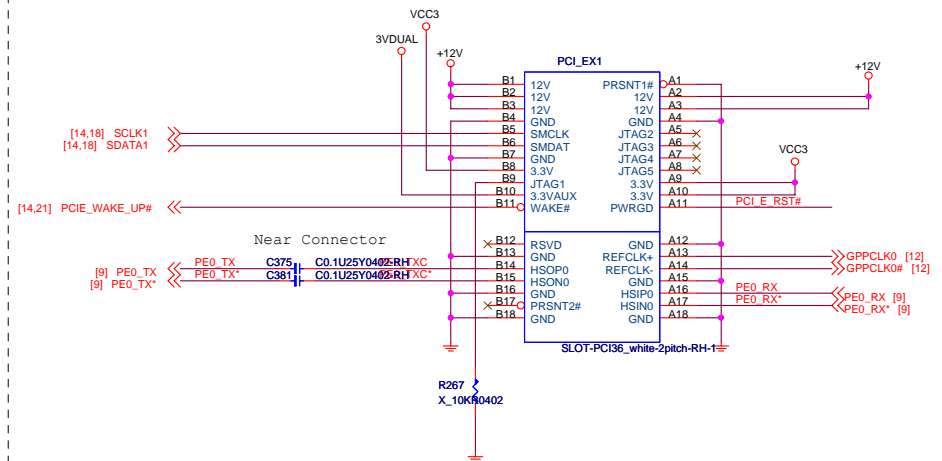
PCI PULL-UP / DOWN RESISTORS



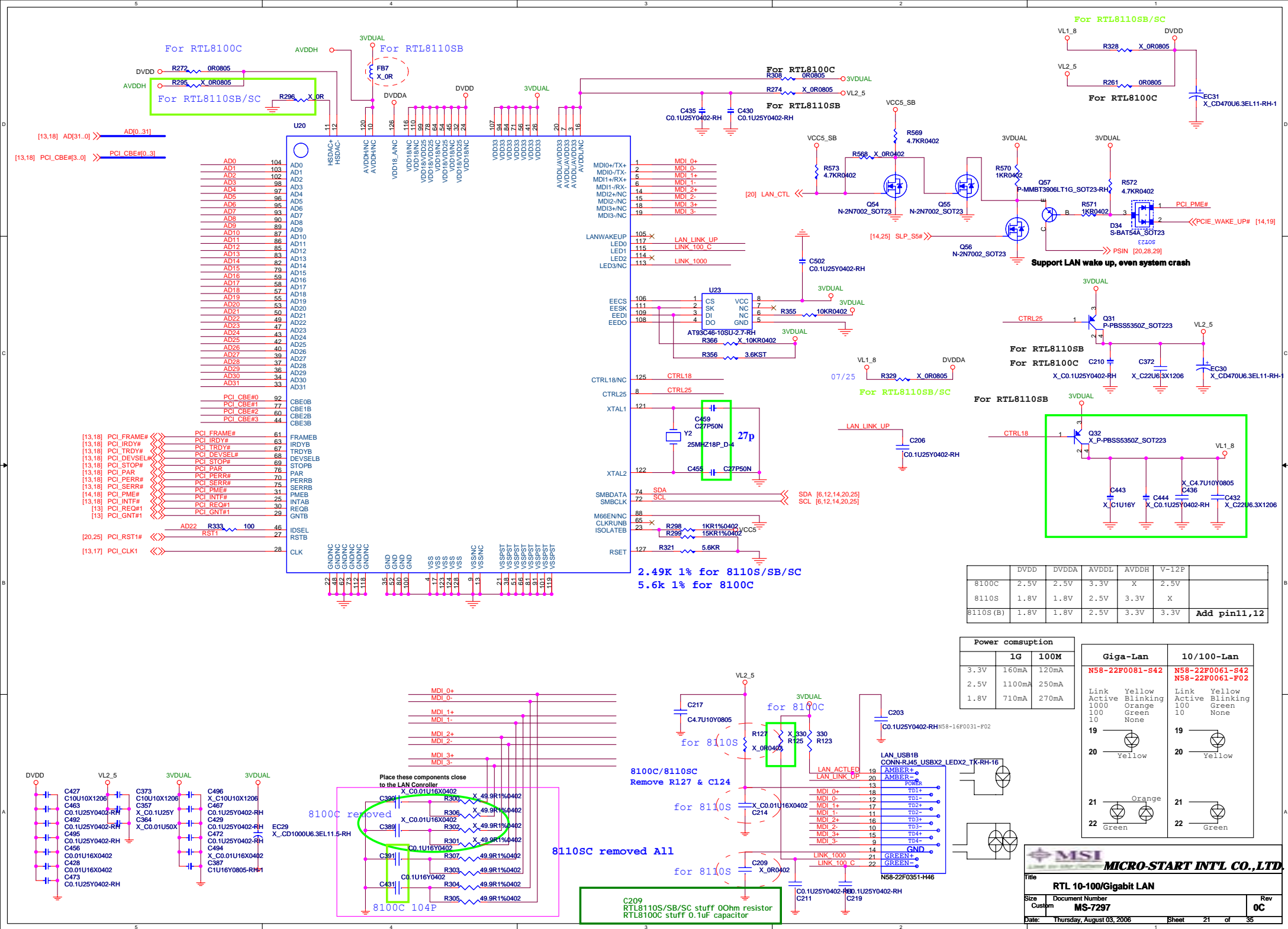
PCI EXPRESS\_16



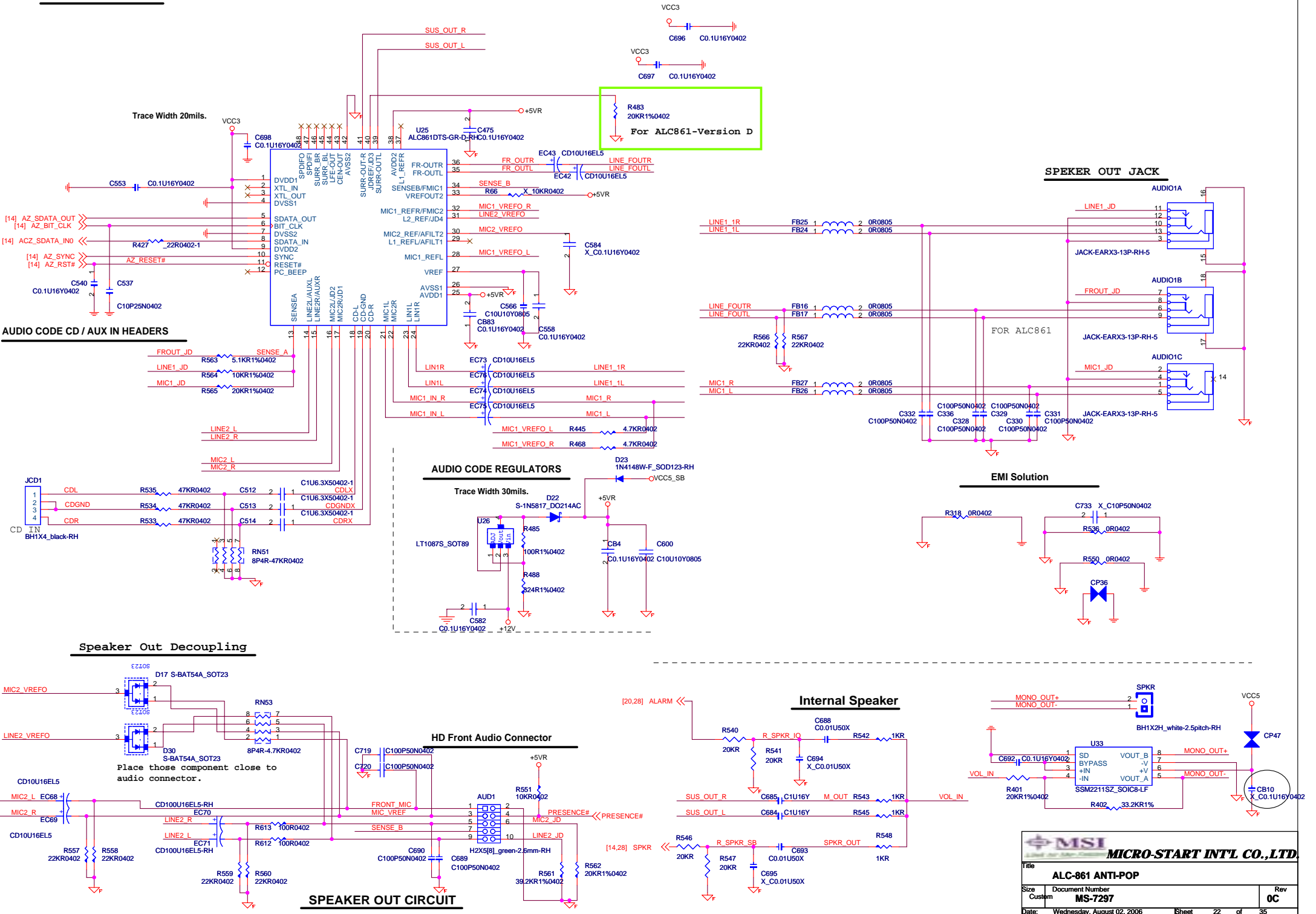
**PCI-Express x1 SLOTT 1**



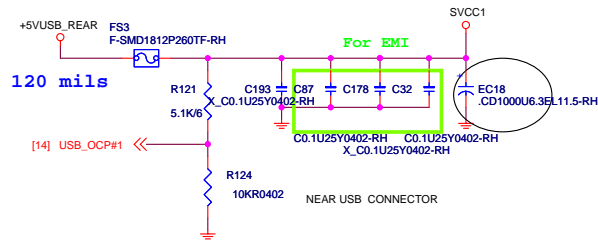




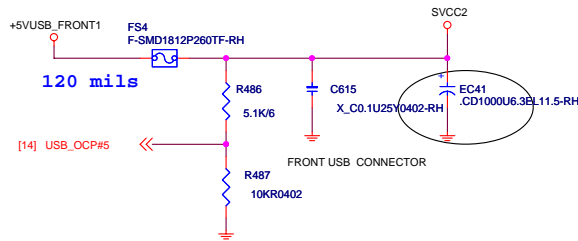
# ALC861 CODEC



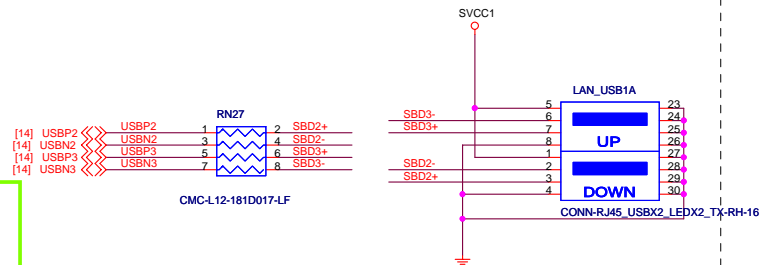
## POWER CIRCUIT FOR USB PORT 0,1



## POWER CIRCUIT FOR USB PORT 4,5,6,7



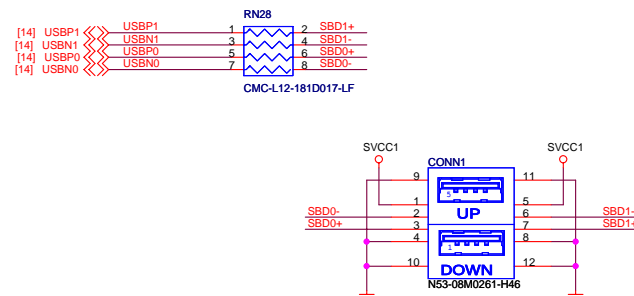
## REAR PANEL USB CONNECTOR FOR USB PORT 0,1



### NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

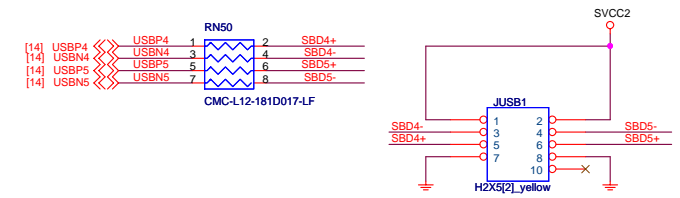
## REAR PANEL USB CONNECTOR FOR USB PORT 2,3



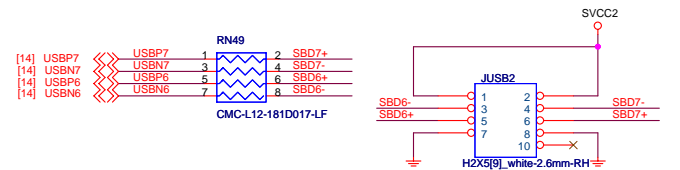
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

## FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

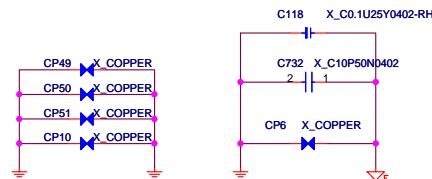
Reserved, can be taken off riser card within bead



## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



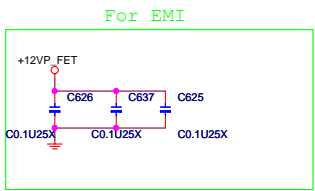
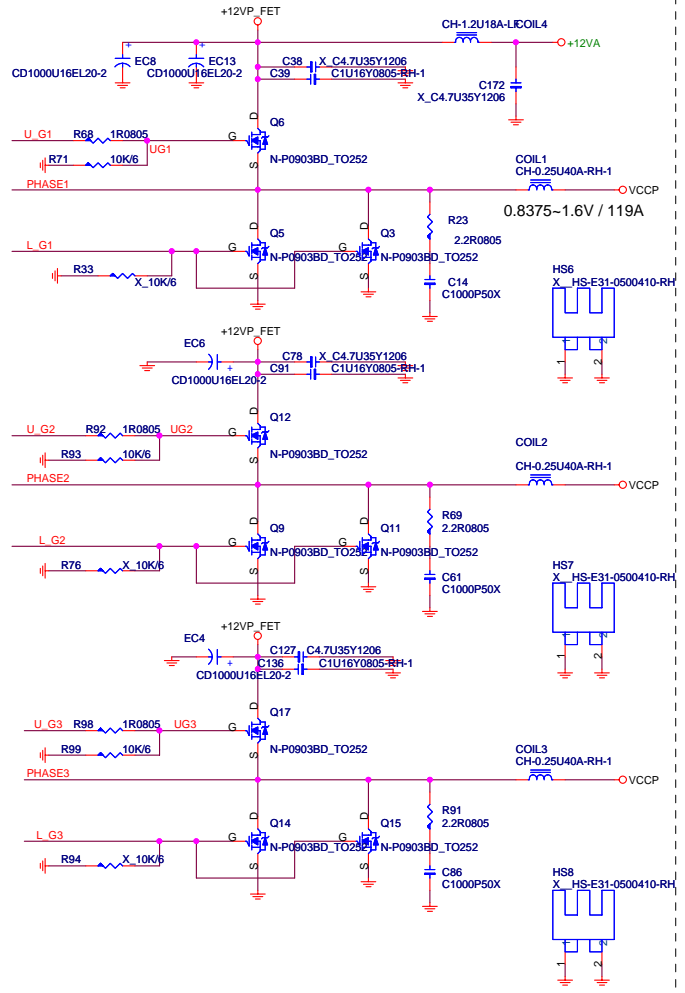
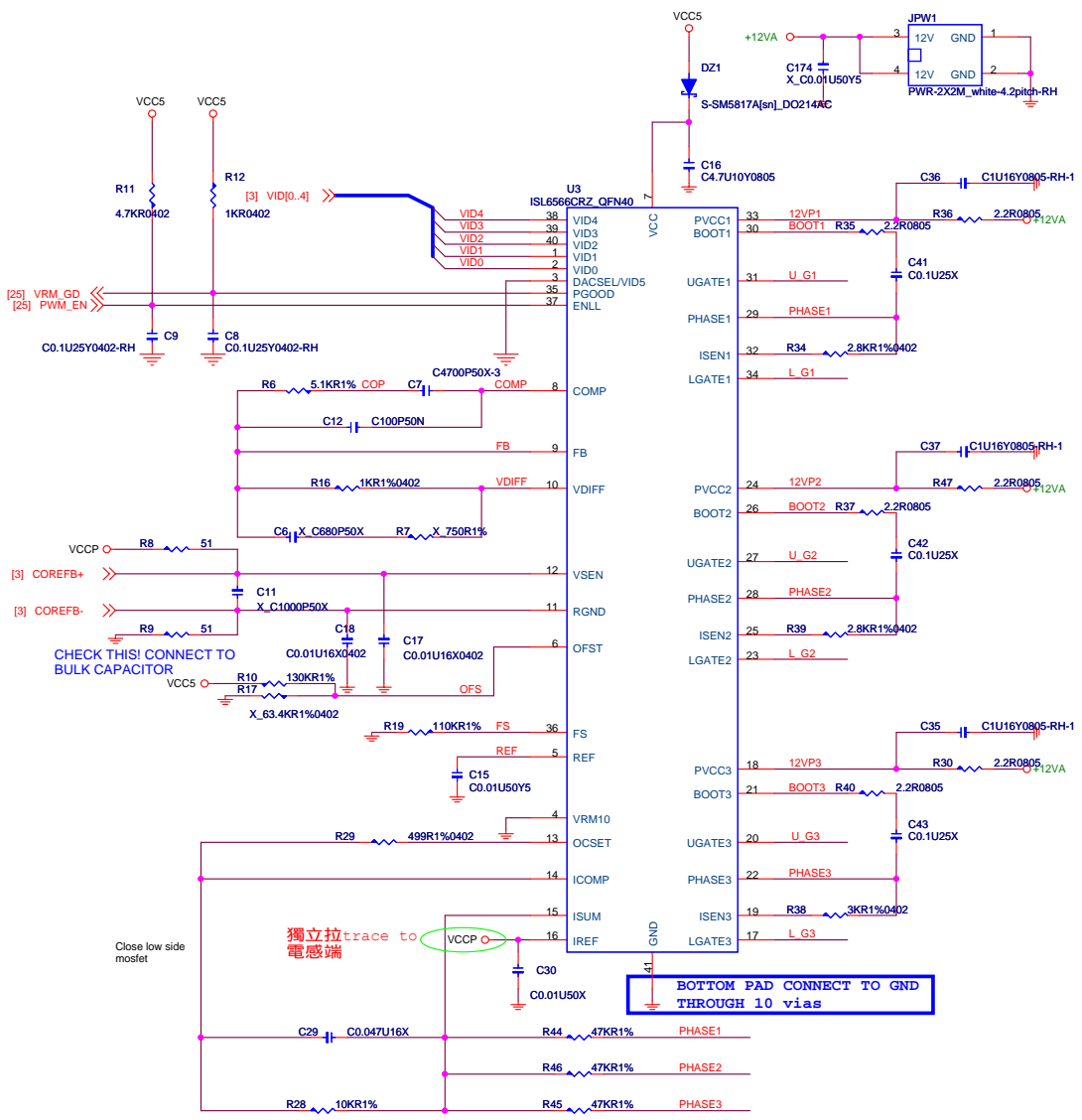
## EMI TEST



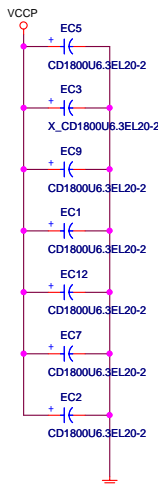


# Voltage Regular Module

IPF06N03LA Rds(on)=8.7mΩ (@4.5V, 30A), Vgs(on)=1.2~2V, Id=50A, Ciss=3110pf, Qg=10nC, Vds=25V, Vgs=±20V  
C100U2SP ESR<13mΩ, Ripple cur.<2.7A, LC<12uA, 105C  
.CD3300U6.3EL25 ESR<12mΩ, Ripplecur.<2800mA, 105C, longlife3000hrs, KZGSeries  
560u\_2.5V ESR=6mΩ, Ripplecur.=4400mA, Lc.<500uA, 105C/2000hrs  
1800UF/6.3V ESR<12mΩ, Ripplecur.<2350mA, 105C, longlife change from 2000hrs to 3000hrs ,KZJ series  
0.6uH/40A 0.6u/20%, Isat=40A, Rdc=1.2m ohm, PEW wire  
CH-1.2U18A 1.2u/20%, Dip-2/vertical7.5mm, 1.2ψ/5.5turns, 18A

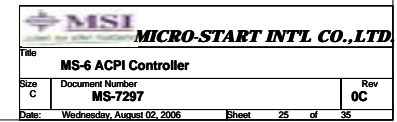


EL Capacitors

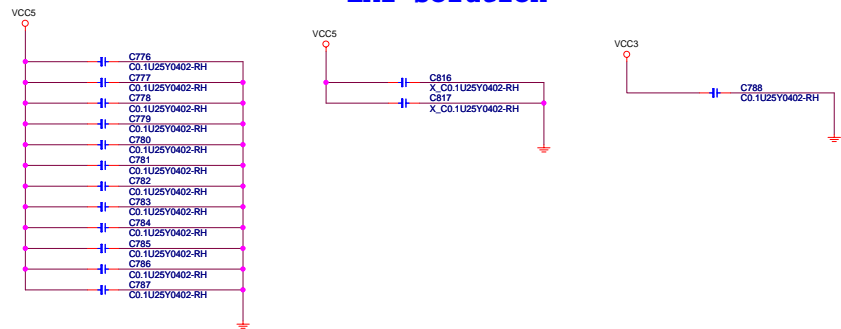




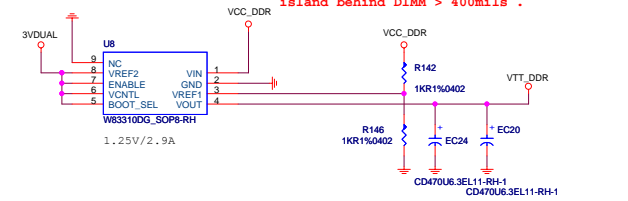
THESE OUTPUT AND INPUT PIN MUST  
BE PULL HIGH



## EMI solution

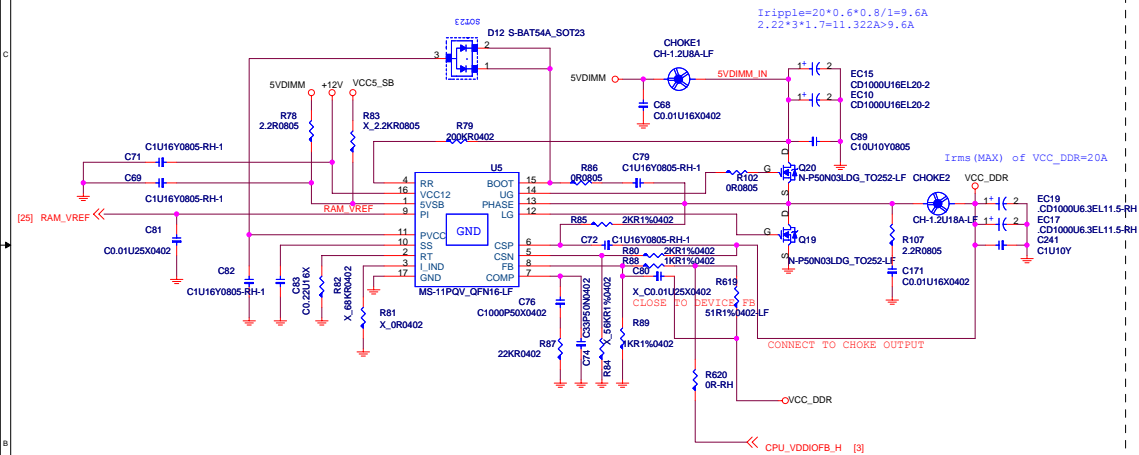


## DDR VTT Power

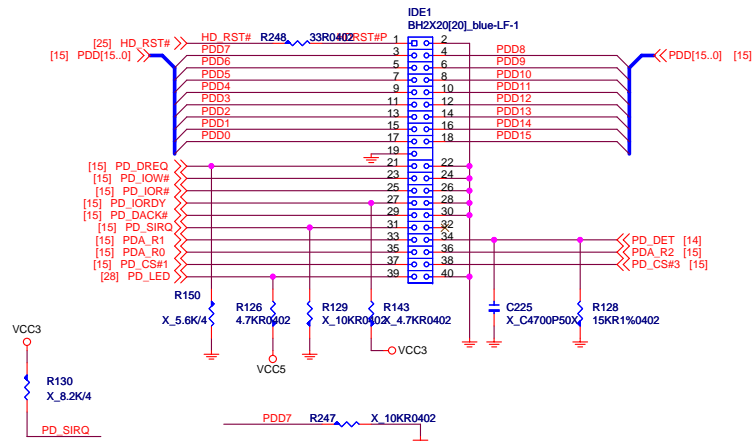


To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

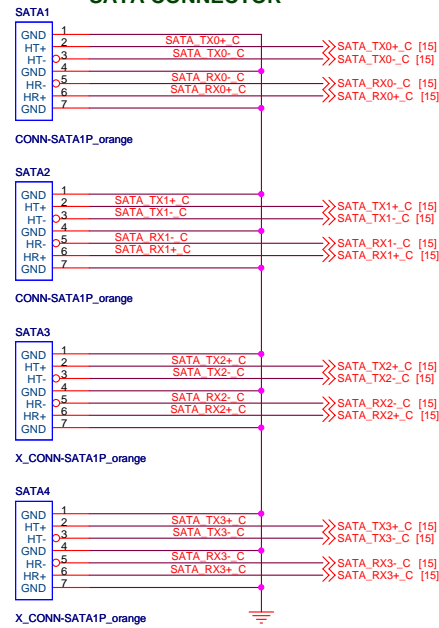
## DDR II 1.8V POWER



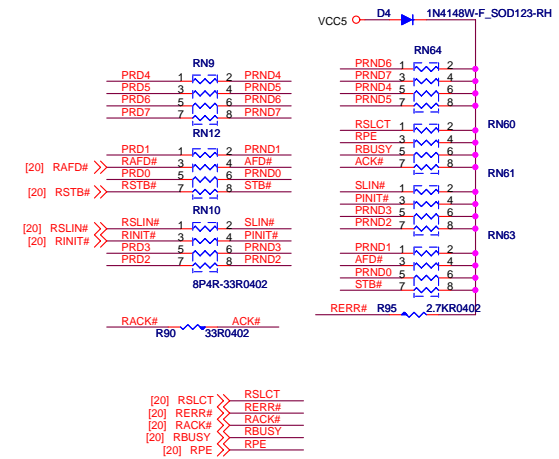
## IDE 1



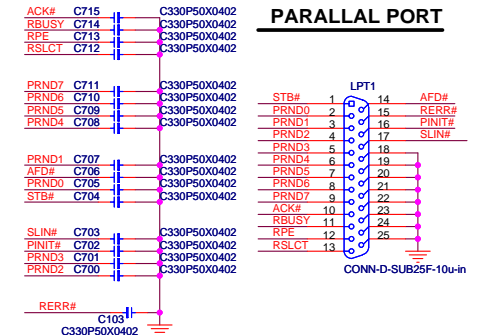
## SATA CONNECTOR



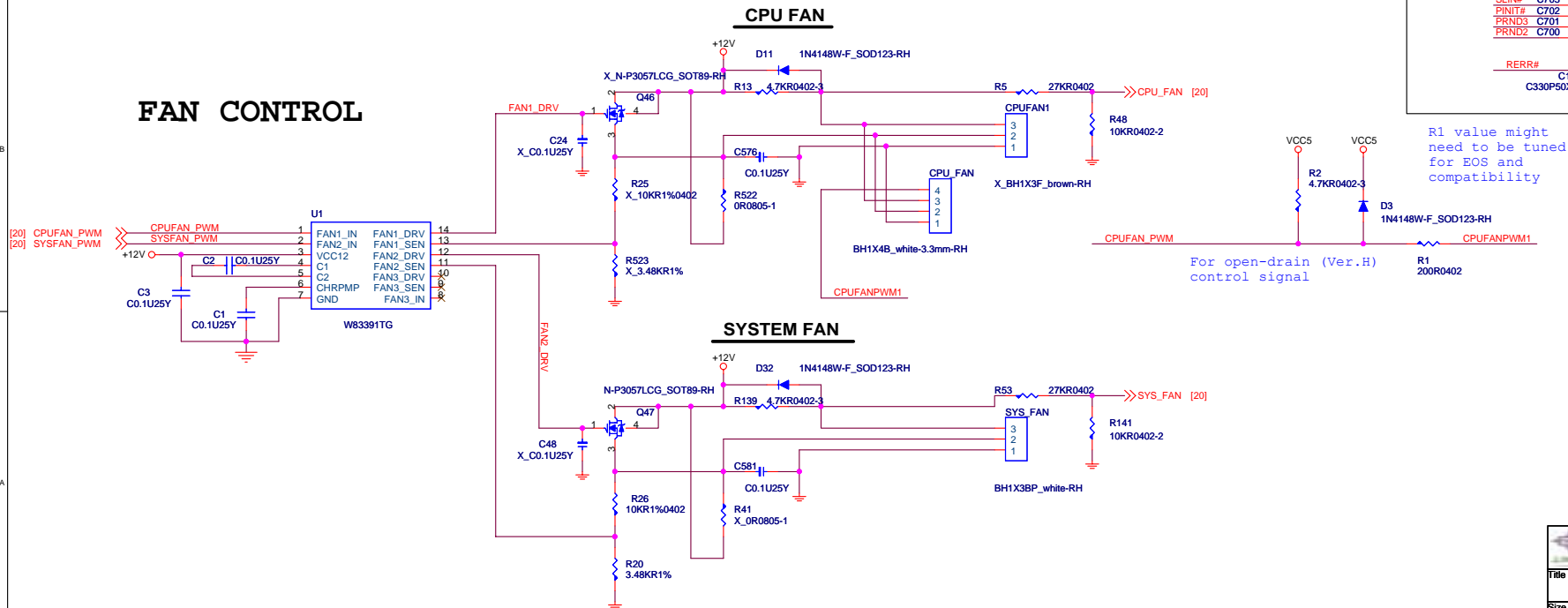
[20] PRD[0..7] >> PRD[0..7]



## PARALLAL PORT



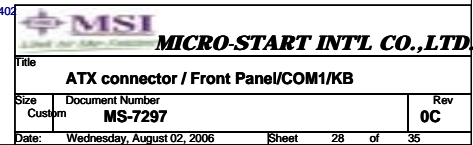
## FAN CONTROL



R1 value might need to be tuned for EOS and compatibility

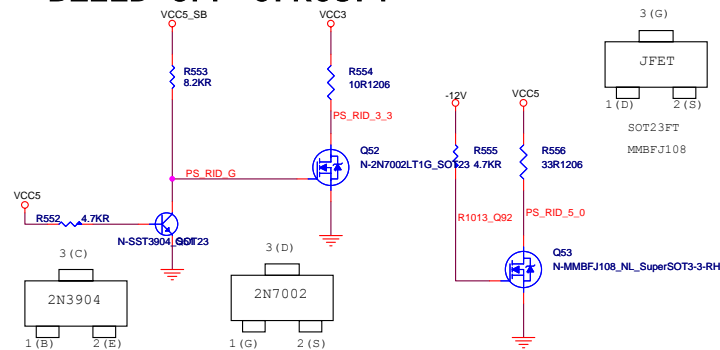
For open-drain (Ver.H) control signal

## Intel Front Panel

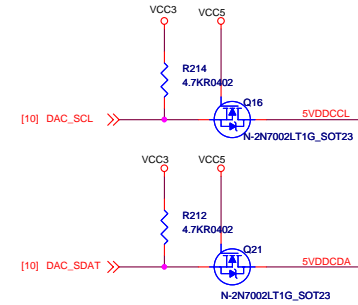
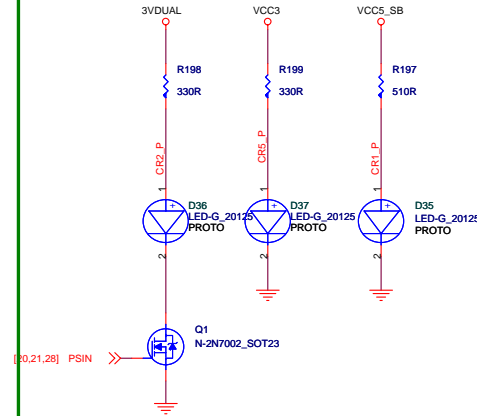
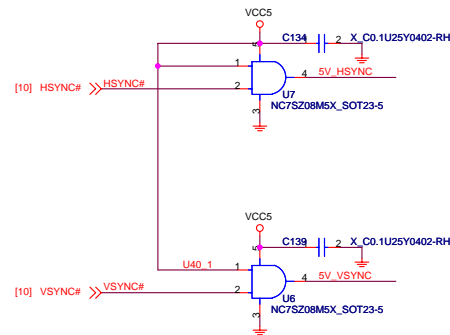


# Near ATX POWER Connector

## BLEED-OFF CIRCUIT

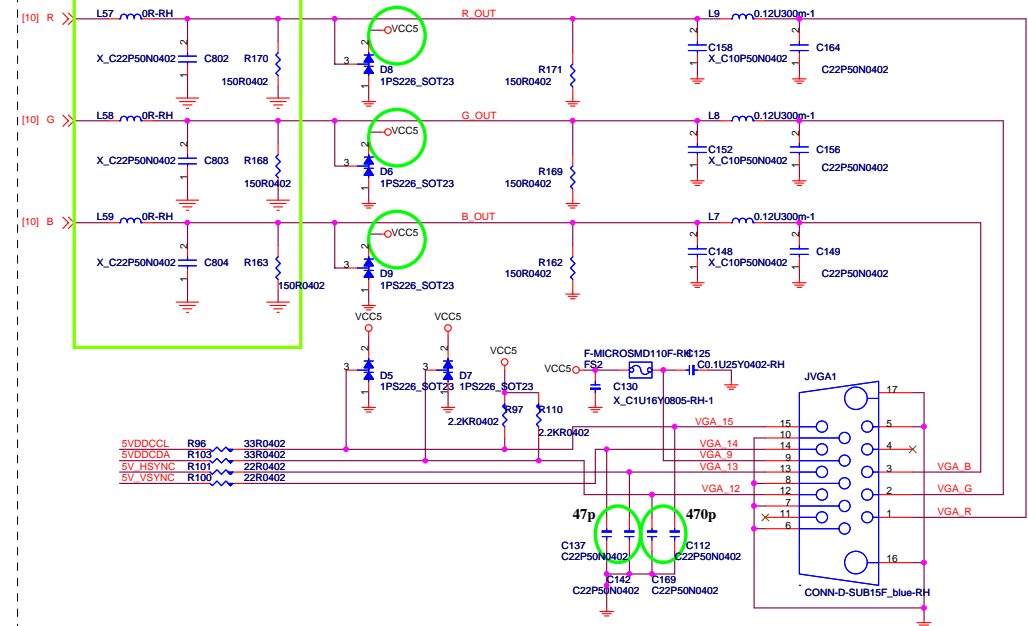


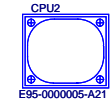
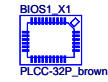
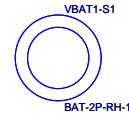
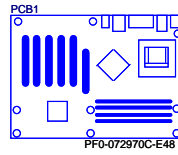
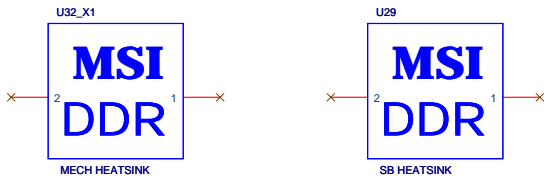
DESIGN NOTE: THIS CIRCUIT IS USED TO BLEED OFF 5.0V & 3.3V



## VGA CONNECTOR

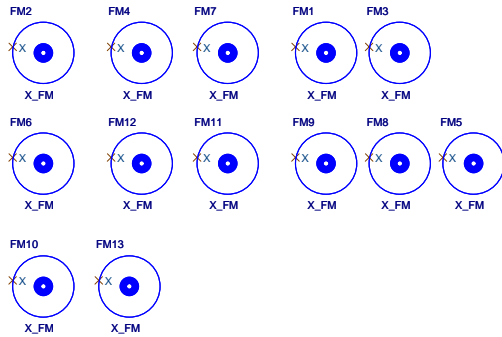
### Closed NB



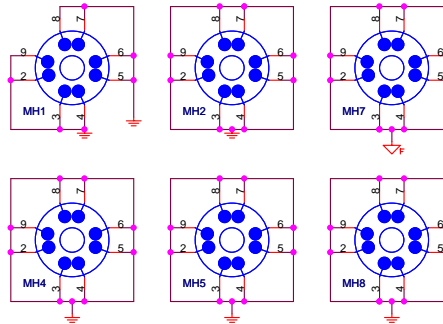


PF0-072970C-E48, 競華, 107, 寶安恩斯通廠 (MSIS)  
PF0-072970C-E48, 競華, 23, 寶安恩斯通廠 (MSIS)  
PF0-072970C-G37, 精成, 107, 寶安恩斯通廠 (MSIS)  
PF0-072970C-G37, 精成, 23, 寶安恩斯通廠 (MSIS)

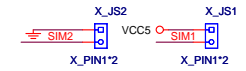
### Optics Orientation Holes



### Mounting Holes



### Simulation



### Model option table

Model type	Function	BOM Config	ERP BOM No.
MS-7297	RS485+SB600+RTL8110SB+ALC861+2PCI+u-ATX +2PS2+8USB+1COM+VGA+1Audio+LPT+RJ45	cfg-7297-0A	601-7297-01S